IES E & T Topic wise Questions

Digital Electronic Circuits

YEAR 1999

MCQ 1

Assertion (A) : A demultiplexer can be used as a decoder.

Reason (R) : A demultiplexer is built by using AND gates only.

(A) Both A & R are true and R is the correct explanation of A

(B) Both A & R are true but R is NOT the correct explanation of A

(C) A is true but R is false

(D) A is false but R is true

MCQ 2

Assertion (A) : The output of an 8-bit A to D converter is 80 H for an input of 2.5 V.

Reason (R) : ADC has an output range of 00 to FFH for an input range of -5 V to $+5$ V.

(A) Both A & R are true and R is the correct explanation of A

(B) Both A & R are true but R is NOT the correct explanation of A

(C) A is true but R is false

(D) A is false but R is true

MCQ 3

The voltage levels of a negative logic system -

(A) Must necessarily be negative

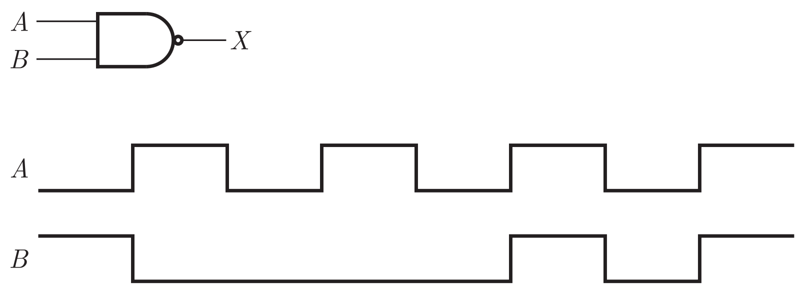
(B) May be negative or positive

(C) Must necessarily be positive

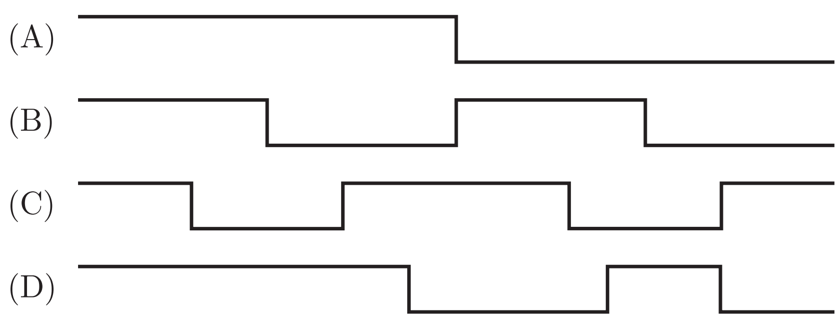
(D) Must be necessarily be 0 V and -5 V

MCQ 4

The given figure shows a NAND gate with input waveforms A and B.

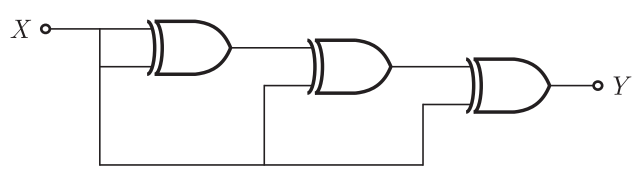


The correct output waveform X of the gate is



MCQ 5

The output Y of the gate circuit is



(A) 1 (B) zero

(C) X (D) $\overline{X}$

MCQ 6

The Boolean theorem $AB + \overline{A}C + BC = AB + \overline{A}C$ corresponds to

(A) $(A+B)\cdot(\overline{A}+C)\cdot(B+C) = (A+B)\cdot(\overline{A}+C)$

(B) $AB + \overline{A}C + BC = AB + BC$

(C) $AB + \overline{A}C + BC = (A + B) \cdot (\overline{A} + C) \cdot (B + C)$

(D) $(A + B) \cdot (\overline{A} + C) \cdot (B + C) = AB + \overline{A}C$

MCQ 7

Match **List-I** (Circuits) with **List-II** (Types of integration level) and select the correct answer using the codes given below the lists :

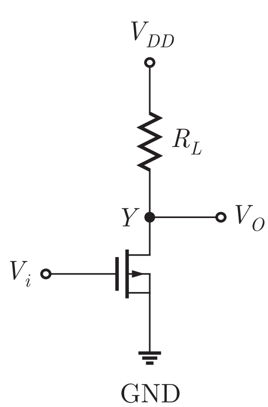
	List I		List II
a.	Full adder	**1.**	VLSI
b.	Magnitude comparator	**2.**	SSI
c.	Programmable logic array	**3.**	MSI

Codes :

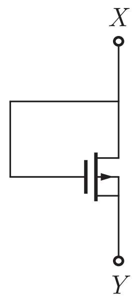
	a	b	c
(A)	2	3	1
(B)	3	2	1
(C)	1	3	2
(D)	2	1	3

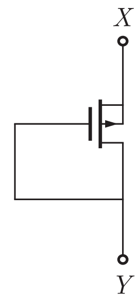
MCQ 8

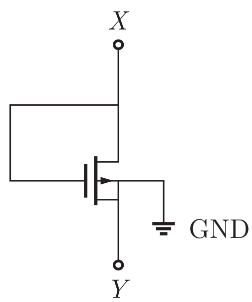
The load resistance R_L between X and Y in the switch shown

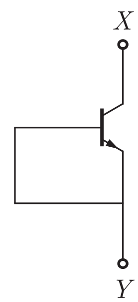


CANNOT be replaced by

(A) 

(B) 

(C) 

(D) 

MCQ 9

$Y = f(A, B) = \Pi \ M(0,1,2,3)$ represents (M is Maxterm)

(A) NOR gate

(B) NAND gate

(C) OR gate

(D) A situation where output is independent of input

MCQ 10

Consider the following statements regarding ICs :

1. ECL has the least propagation delay.
2. TTL has the largest fanout.
3. CMOS has the biggest noise margin.
4. TTL has the lowest power consumption.

Which of these statements are correct ?

(A) 1 and 3 (B) 2 and 4

(C) 3 and 4 (D) 1 and 2

MCQ 11

For a logic family -

V_{OH} is the minimum output high level voltage.

V_{OL} is the maximum output low level voltage.

V_{IH} is the minimum acceptable input high level voltage.

V_{IL} is the maximum acceptable input low level voltage.

The correct relationship among these is

(A) $V_{IH} > V_{OH} > V_{IL} > V_{OL}$

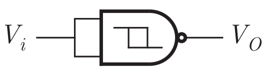
(B) $V_{OH} > V_{IH} > V_{IL} > V_{OL}$

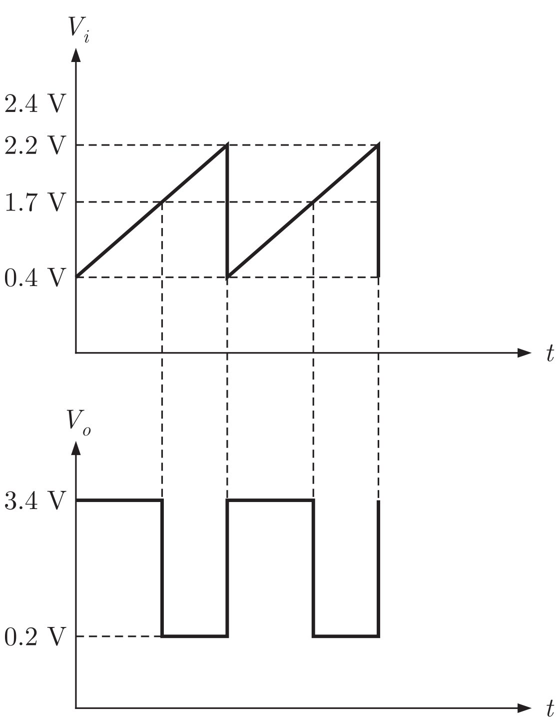
(C) $V_{IH} > V_{OH} > V_{OL} > V_{IL}$

(D) $V_{OH} > V_{IH} > V_{OL} > V_{IL}$

MCQ 12

The input waveform V_i and the output waveform V_O of a Schmitt NAND are shown in the given figures.





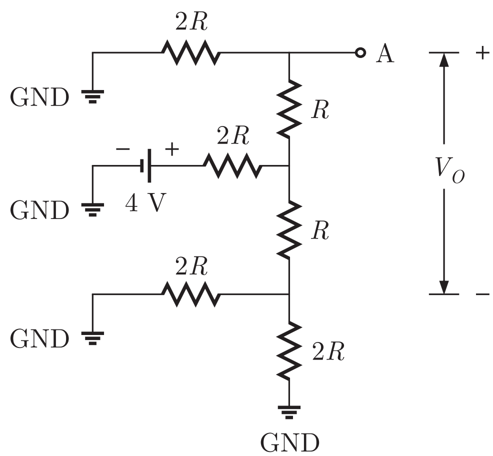
The duty cycle of the output waveform will be

(A) 100 % (B) 85.5 %

(C) 72.2 % (D) 25 %

MCQ 13

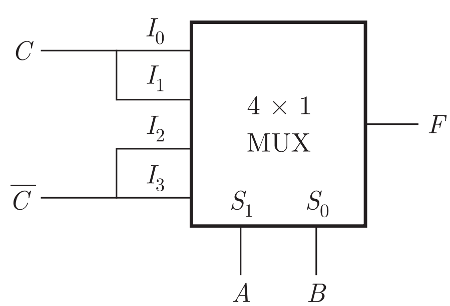
The output voltage V_O with respect to ground of the R-$2R$ ladder network shown is



(A) 1 V (B) 2 V
(C) 3 V (D) 4 V

MCQ 14

The logic circuit realized by the circuit shown in the given figure will be



(A) $B \odot C$ (B) $B \oplus C$
(C) $A \odot C$ (D) $A \oplus C$

MCQ 15

In a negative edge triggered J-K flip-flop, in order to have the output Q state 0, 0 and 1 in the next three successive clock pulses, the J-K

input states required would be respectively

(A) 00, 00 and 10 (B) 00, 01 and 11

(C) 00, 10 and 11 (D) 01, 10 and 11

MCQ 16

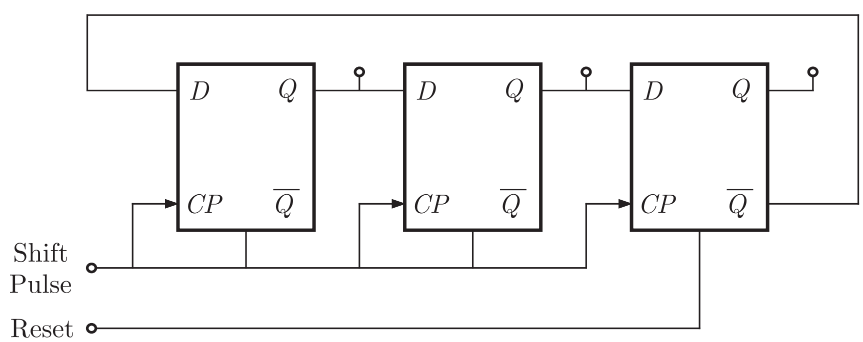
The initial state of MOD-16 down counter is 0110. After 37 clock pulses, the state of the counter will be

(A) 1011 (B) 0110

(C) 0101 (D) 0001

MCQ 17

A three-bit register is shown



To have the content '000' again, the number of clock pulses required would be

(A) 3 (B) 6

(C) 8 (D) 16

MCQ 18

Symmetrical square wave of time period 100 μs can be obtained from square wave of time period 10 μs by using a

(A) Divide by - 5 circuit

(B) Divide by - 2 circuit

(C) Divide by - 5 circuit followed by a divide by - 2 circuit

(D) BCD counter

MCQ 19

A 1 μs pulse can be converted into a 1 ms pulse by using

(A) A monostable multivibrator

(B) An astable multivibrator

(C) A bistable multivibrator

(D) A J-K flip-flop

MCQ 20

For a particular type of memory, the access time and the cycle time are respectively 200 ns and 200 ns. The maximum rate at which the data can be accessed, is

(A) 2.5×10^6/s

(B) 5×10^6/s

(C) 0.2×10^6/s

(D) 10^6/s

YEAR 2000

MCQ 21

The minimum decimal equivalent of the number 11C.0 is

(A) 183

(B) 194

(C) 268

(D) 269

MCQ 22

$(FE35)_{16}$ XOR $(CB15)_{16}$ is equal to

(A) $(3320)_{16}$

(B) $(FF35)_{16}$

(C) $(FF50)_{16}$

(D) $(3520)_{16}$

MCQ 23

Assertion (A) : Schottky transistors are preferred over normal transistor in digital circuits.

Reason (R) : Schottky transistor operate in active and saturation regions.

(A) Both A & R are true and R is the correct explanation of A

(B) Both A & R are true but R is NOT the correct explanation of A

(C) A is true but R is false

(D) A is false but R is true

MCQ 24

Assertion (A) : A ring counter is preferred over a binary sequential counter.

Reason (R) : The decoding logic is simple for a ring counter.

(A) Both A & R are true and R is the correct explanation of A

(B) Both A & R are true but R is NOT the correct explanation of A

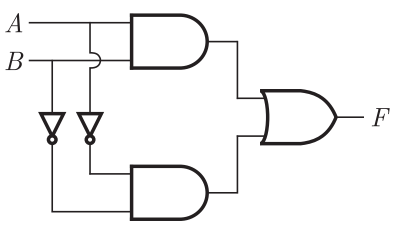
(C) A is true but R is false

(D) A is false but R is true

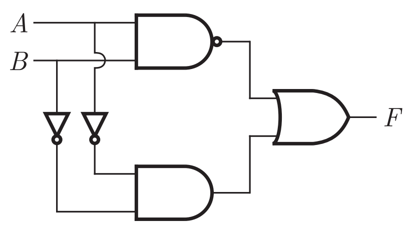
MCQ 25

Which one of the following represents the coincides logic ?

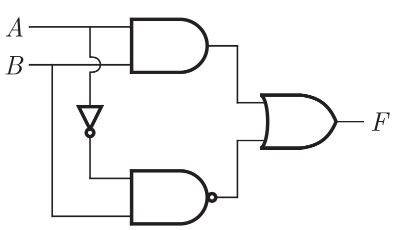
(A)



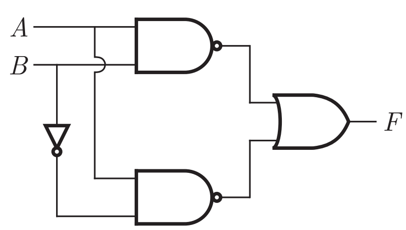
(B)



(C)



(D)



MCQ 26

A T flip-flop function is obtained from a J-K flip-flop. If the flip-flop belongs to a TTL family, the connection needed at the input must be

(A) $J = K = 1$

(B) $J = K = 0$

(C) $J = 1$ and $K = 0$

(D) $J = 0$ and $K = 1$

MCQ 27

Karnaugh map is used to

(A) Minimise the number of flip-flops in a digital circuit

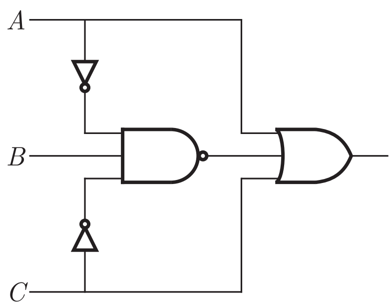
(B) Minimise the number of gates only in a digital circuit

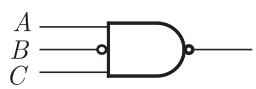
(C) Minimise the number of gates and fan-in of a digital circuit

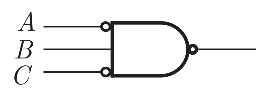
(D) Design gates

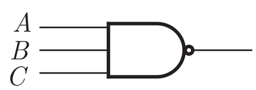
MCQ 28

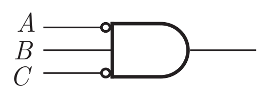
Which one of the following circuits is the minimised logic circuit for the circuit shown



(A) 

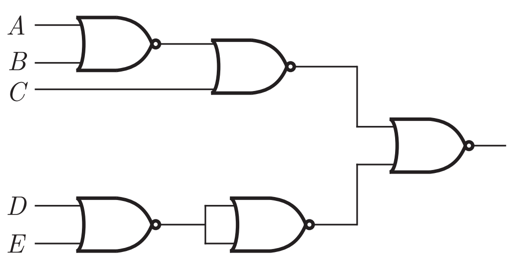
(B) 

(C) 

(D) 

MCQ 29

The circuit shown realizes the function



(A) $(\overline{A+B}+C)(\overline{D}\,\overline{E})$

(B) $(\overline{A+B}+C)(D\overline{E})$

(C) $(A+\overline{B+C})(\overline{D}\,E)$

(D) $(A+B+\overline{C})(\overline{D}\,\overline{E})$

MCQ 30

The logic operations of two combinational circuits given in **Figure - I** and **Figure - II** are

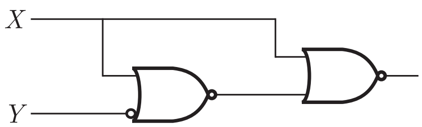


Figure - I

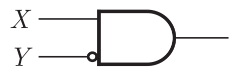


Figure - II

(A) Entirely different
(B) Identical
(C) Complementary
(D) Dual

MCQ 31

The figure of merit of a logic family is given by

(A) Gain $\times$ Bandwidth
(B) Propagation delay time $\times$ Power dissipation
(C) Fan-out $\times$ Propagation delay time
(D) Noise margin $\times$ Power dissipation

MCQ 32

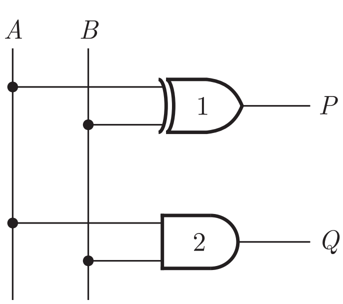
Which of the following statements correctly defines the full-adder ?

An adder circuit

(A) Having two inputs used to add two binary digits. It produces their sum and carry as input.
(B) Having three inputs used to add two binary digits plus a carry. It produces their sum and carry as outputs.
(C) Used in the least significant position when adding two binary digits with no carry-in to consider. It produces their sum and carry as outputs.
(D) Having two inputs and two outputs.

MCQ 33

The half-adder circuit in the given figure has inputs $AB = 11$



The logic level of P and Q outputs will be

(A) $P = 0$ and $Q = 0$
(B) $P = 0$ and $Q = 1$
(C) $P = 1$ and $Q = 0$
(D) $P = 1$ and $Q = 1$

MCQ 34

Which one of the following can be used as parallel to series converter ?

(A) Decoder
(B) Digital counter
(C) Multiplexer
(D) Demultiplexer

MCQ 35

Consider the following statements :

A multiplexer

1. Selects one of the several inputs and transmits it to a single output.
2. Routes the data from a single input to one of many output.
3. Converts parallel data into serial data.
4. Is a combinational circuit.

Which of these statements are correct ?

(A) 1, 2 and 4
(B) 2, 3 and 4
(C) 1, 3 and 4
(D) 1, 2 and 3

MCQ 36

Consider the following statements :

1. Race around condition occurs in a J-K flip-flop when both the inputs are one.
2. A flip-flop is used to store one bit of information.
3. A transparent latch consists of a D type flip-flop.
4. Master-slave configuration is used in flip-flops to store two bits of information.

Which of these statements are correct ?

(A) 1, 2 and 3
(B) 1, 3 and 4
(C) 1, 2 and 4
(D) 2, 3 and 4

MCQ 37

A ring counter consisting of five flip-flops will have

(A) 5 states
(B) 10 states
(C) 32 states
(D) Infinite states

MCQ 38

A crystal oscillator is frequently used in digital circuits for timing purposes because of its

(A) Low cost
(B) High frequency stability
(C) Simple circuitry
(D) Ability of set the frequency at the desired value

MCQ 39

Which one of the following statements is correct ?

(A) RAM is a non-volatile memory whereas ROM is a volatile memory.
(B) RAM is a volatile memory whereas ROM is a non-volatile memory.
(C) Both RAM and ROM are volatile memories but in ROM data is not lost when power is switched off.
(D) Both RAM and ROM are non-volatile memories but in RAM data is lost when power is switched off.

MCQ 40

Match **List - I** (Memory elements) with **List - II** (Properties) and select the correct answer using the codes given below the lists :

	List - I		**List - II**
a.	Semiconductor memory	**1.**	Destructive readout
b.	Ferrite core memory	**2.**	Combinational logic
c.	Magnetic tape memory	**3.**	Volatile

Codes :

a	b	c

(A)	2	1	3
(B)	1	3	2
(C)	3	2	1
(D)	3	1	2

YEAR 2001

MCQ 41

F's complement of $(2BFD)_{Hex}$ is

(A) E304
(B) D403
(C) D402
(D) C403

MCQ 42

The number of digit 1 present in the binary representation of $3 \times 512 + 7 \times 64 + 5 \times 8 + 3$ is

(A) 8
(B) 9
(C) 10
(D) 12

MCQ 43

The output voltage of a 5-bit D/A binary ladder that has a digital input of 11010 (Assuming $0 = 0\text{ V}$ and $1 = +10\text{ V}$)

(A) 3.4375 V
(B) 6.0 V
(C) 8.125 V
(D) 9.6875 V

MCQ 44

The 54/74164 chip is an 8-bit serial-input-parallel-output shift register. The clock is 1 MHz. The time needed to shift an 8-bit binary number into the chip is

(A) 1 μs
(B) 2 μs
(C) 8 μs
(D) 16 μs

MCQ 45

Assertion (A) : A look-ahead carry adder is a fast adder.

Reason (R) : A parallel carry adder generates sum digits directly

from the input digits.

(A) Both A & R are true and R is the correct explanation of A

(B) Both A & R are true but R is NOT the correct explanation of A

(C) A is true but R is false

(D) A is false but R is true

MCQ 46

Assertion (A) : Master-slave *J-K* flip-flop is free from race-around condition.

Reason (R) : Master-slave uses two *J-K* flip-flop.

(A) Both A & R are true and R is the correct explanation of A

(B) Both A & R are true but R is NOT the correct explanation of A

(C) A is true but R is false

(D) A is false but R is true

MCQ 47

Assertion (A) : ECL gate has the highest speed of operation as compared to other logic families.

Reason (R) : ECL gate dissipates more power.

(A) Both A & R are true and R is the correct explanation of A

(B) Both A & R are true but R is NOT the correct explanation of A

(C) A is true but R is false

(D) A is false but R is true

MCQ 48

Consider the following logic families :

1. MOS 2. DTL

3. RTL 4. ECL

The sequence of these logic families in the order of their increasing noise margin is

(A) 3, 4, 1, 2 (B) 3, 4, 2, 1

(C) 4, 3, 1, 2 (D) 4, 3, 2, 1

MCQ 49

An 8-bit D/A converter has a full scale output voltage of 20 V. The output voltage when the input is 11011011, is

(A) 160 mV
(B) 78 mV
(C) 20 V
(D) 17 V

MCQ 50

In the negative logic system,

(A) The more negative of the two logic levels represents a logic '1' state
(B) The more negative of the two logic levels represents a logic '0' state
(C) All input and output voltage levels are negative
(D) The output is always complement of the intended logic function

MCQ 51

If the output of a logic gate is '1' when all its inputs are at logic '0', the gate is either

(A) A NAND or NOR
(B) An AND or an Ex-NOR
(C) An NOR or an NAND
(D) An Ex-OR or an Ex-NOR

MCQ 52

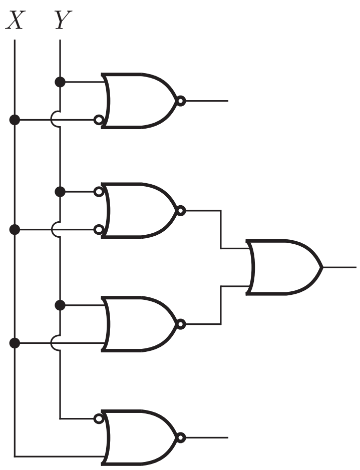
For the karnaugh map shown in the figure, the minimum boolean function is

$yz \backslash x$	0	1
00	1	1
01	1	
11	1	1
10	1	1

(A) $x'y' + z' + yz$
(B) $xz' + z + zy'$
(C) $xy + z + y'z$
(D) $x'z + z' + yz$

MCQ 53

The circuit shown in the given fig. is



(A) An adder circuit
(B) A substractor circuit
(C) A comparator circuit
(D) A parity generator circuit

MCQ 54

Which one of the following is equivalent to the boolean expression $Y = \overline{A}\,\overline{B} + \overline{B}\,\overline{C} + \overline{C}\,\overline{A}$?

(A) $\overline{AB + BC + CA}$
(B) $(\overline{A} + \overline{B})(B + \overline{C})(\overline{A} + \overline{C})$
(C) $\overline{(A + B)(B + C)(C + A)}$
(D) $\overline{(A + B)}\,\overline{(B + C)}\,\overline{(C + A)}$

MCQ 55

Given boolean theorem

$AB + \overline{A}C + BC = AB + \overline{A}C$

Which one of the following identities is true ?

(A) $(A + B) \cdot (\overline{A} + C) \cdot (B + C) = (A + B) \cdot (\overline{A} + C)$
(B) $AB + \overline{A}C + BC = AB + BC$
(C) $AB + \overline{A}C + BC = (A + B) \cdot (\overline{A} + C) \cdot (B + C)$
(D) $(A + B) \cdot (\overline{A} + C) \cdot (B + C) = AB + \overline{A}C$

MCQ 56

The number of 4-line-to-16-line decoders required to make an 8-line-

to-256-line decoder is

(A) 16 (B) 17

(C) 32 (D) 64

MCQ 57

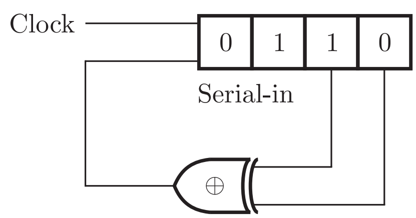
The characteristic equation of the T flip-flop is given by

(A) $Q^+ = TQ + \overline{T}\,\overline{Q}$ (B) $Q^+ = T\overline{Q} + Q\overline{T}$

(C) $Q^+ = T + Q$ (D) $Q^+ = T\overline{Q}$

MCQ 58

The initial contents of the 4-bit serial-in-parallel-out, right shift, shift register shown are 0110. After three clock pulses are applied, the contents of the shift register will be



(A) 0000 (B) 0101

(C) 1010 (D) 1111

MCQ 59

Four memory chips of 16×4 size have their address buses connected together. This system will be of size

(A) 64×4 (B) 16×16

(C) 32×8 (D) 256×1

YEAR 2002

MCQ 60

A typical cell, for a dynamic RAM can be implemented by using how many MOS transistor ?

(A) Six (B) Five

(C) One (D) Two

MCQ 61

Assertion (A) : Master-slave J-K flip-flop is preferred to an edge-triggered J-K flip-flop in high speed circuits.

Reason (R) : Master-slave J-K flip-flop is free from race-around problem.

(A) Both A & R are true and R is the correct explanation of A

(B) Both A & R are true but R is NOT the correct explanation of A

(C) A is true but R is false

(D) A is false but R is true

MCQ 62

In signed magnitude representation, the binary equivalent of 22.5625 is (the bit before comma represents the sign)

(A) 0, 10110.1011 (B) 0,10110.1001

(C) 1, 10101.1001 (D) 1, 10110.1001

MCQ 63

Which of the following represents $E3_{16}$?

(A) $(1CE)_{16} + (A2)_{16}$ (B) $(1BC)_{16} - (DE)_{16}$

(C) $(2BC)_{16} - (1DE)_{16}$ (D) $(200)_{16} - (11D)_{16}$

MCQ 64

The open collector output of two 2-input NAND gates are connected to a common pull-up resistor. If the inputs of the gates are A, B and C, D respectively, the output is equal to

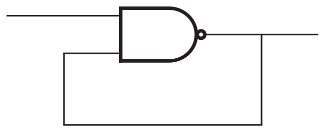
(A) $\overline{AB} \cdot \overline{CD}$ (B) $\overline{AB} + \overline{CD}$

(C) $AB + CD$ (D) $AB \cdot CD$

MCQ 65

Consider the following digital circuits :

1. Multiplexers
2. Read Only Memories
3. D - latch
4. Circuit as shown



Which of these come under the class of combinational of circuits ?

(A) 1 and 2
(B) 3 and 4
(C) 1, 2 and 3
(D) 1, 2, 3 and 4

MCQ 66

With 4 boolean variables, how many boolean expressions can be formed ?

(A) 16
(B) 256
(C) 1024 (1 K)
(D) 64 K (64×1024)

MCQ 67

Match **List - I** (Logic gates) with **List - II** (Operation) and select the correct answer using the codes given below the lists :

	List - I		List - II
a.	TTL	**1.**	More logical swing
b.	ECL	**2.**	Low power dissipation
c.	HTL	**3.**	Current hogging
d.	CMOS	**4.**	NOR/OR output
		5.	Totem-pole output

Codes :

	a	b	c	d
(A)	3	2	5	1
(B)	3	2	4	5
(C)	2	3	4	5
(D)	2	3	5	1

MCQ 68

How is inversion achieved using Ex-OR gate ?

(A) Giving input signal to the two input lines of the gate tied together

(B) Giving input to one input line and logic zero to the other line

(C) Giving input to one input line and logic one to the other line

(D) Inversion cannot be achieved using Ex-OR gate

MCQ 69

Match **List - I** (Logic type) with **List - II** (Power dissipation per gate in mW) and select the correct answer using the codes given below the lists :

	List - I		List - II
a.	DTL	**1.**	55
b.	TTL	**2.**	10
c.	ECL	**3.**	8
d.	MOS	**4.**	1
		5.	40

Codes :

	a	b	c	d
(A)	3	5	4	2
(B)	1	2	5	4
(C)	3	2	5	4
(D)	1	5	4	2

MCQ 70

Figure I, II and III show different faces of a dice. The symbol at the bottom of Figure III is

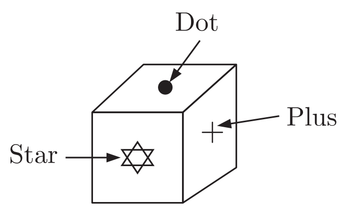


Figure I

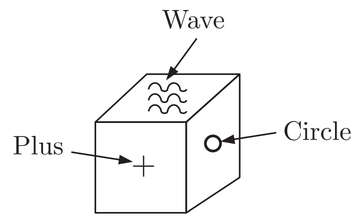


Figure II

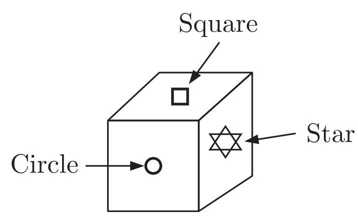


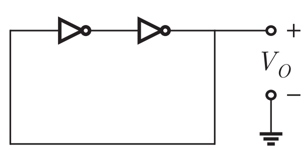
Figure III

(A) Plus
(B) Dot
(C) Wave
(D) Square

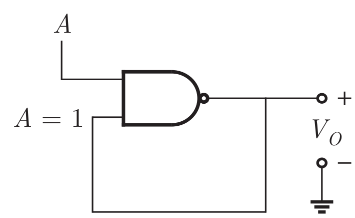
MCQ 71

Consider the following circuits (Assume all gates to have a finite propagation delay) :

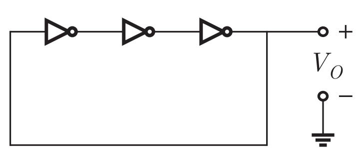
(1)



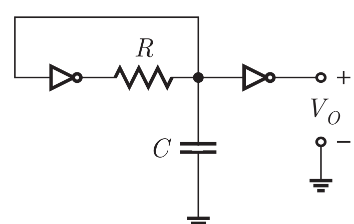
(2)



(3)



(4)



Which of these circuits generate a periodic square wave output ?

(A) 1 and 2
(B) 3 and 4
(C) 2, 3 and 4
(D) 1, 2, 3 and 4

MCQ 72

The minimized expression for the given K-map (X : don't care) is

CD \ AB	00	01	11	10
00	0	0	1	1
01	0	X	X	1
11	X	X	1	X
10	1	0	1	1

(A) $A+\overline{B}C$
(B) $B+AC$
(C) $C+AB$
(D) ABC

MCQ 73

Consider the boolean expression

$$X = ABCD + A\overline{B}CD + \overline{A}BCD + \overline{A}C\overline{B}D$$

The simplified form of X is

(A) $\overline{C}+\overline{D}$
(B) BC
(C) CD
(D) BC

MCQ 74

Which of the following is a self-complementing code ?

(A) 8421 code
(B) Excess-3 code
(C) Pure binary code
(D) Gray code

MCQ 75

Match **List - I** with **List - II** and select the correct answer using the codes given below the lists :

	List - I		List - II
a.	TTL	**1.**	Low propagation delay
b.	ECL	**2.**	Low power consumption

c.	MOS	**3.**	Higher packing density of Si wafer
d.	CMOS	**4.**	Saturated bipolar logic
		5.	High fan-out

Codes :

	a	b	c	d
(A)	4	1	3	2
(B)	5	3	2	1
(C)	4	3	2	1
(D)	5	1	3	2

MCQ 76

A sequence detector is required to give a logical output of 1 whenever the sequence 1011 is detected in the incoming pulse stream. Minimum number of flip-flops needed to build the sequence detector is

(A) 4 (B) 3

(C) 2 (D) 1

MCQ 77

A number is expressed in binary two's complement as 10011. Its decimal equivalent value is

(A) 19 (B) 13

(C) -19 (D) -13

YEAR 2003

MCQ 78

The output of a logic gate is '1' when all its inputs are '0'. Then the gate is either

(A) A NAND or an Ex-OR gate

(B) A NOR or an Ex-NOR gate

(C) An OR or an Ex-NOR gate

(D) An AND or an Ex-OR gate

MCQ 79

Match **List - I** with **List - II** and select the correct answer using the codes given below the lists :

	List - I		List - II
a.	$A \oplus B = 0$	**1.**	$A \neq B$
b.	$\overline{A + B} = 0$	**2.**	$A = B$
c.	$\overline{A} \cdot B = 0$	**3.**	$A = 1$ or $B = 1$
d.	$A \oplus B = 1$	**4.**	$A = 1$ or $B = 0$

Codes :

	a	b	c	d
(A)	3	2	1	4
(B)	2	3	4	1
(C)	3	2	4	1
(D)	2	3	1	4

MCQ 80

The boolean expression $(\overline{A} + B)(A + \overline{C})(\overline{B} + \overline{C})$ simplifies to

(A) $(A + B)\overline{C}$
(B) $(A + \overline{B})\overline{C}$
(C) $(\overline{A} + B)\overline{C}$
(D) $(\overline{A} + \overline{B})\overline{C}$

MCQ 81

The minimum number of NAND gates required to implement the boolean function $A + A\overline{B} + A\overline{B}C$ is equal to

(A) Zero
(B) 1
(C) 4
(D) 7

MCQ 82

The addition of two binary variables A and B results into a SUM and CARRY output. Consider the following expressions for the SUM and CARRY outputs.

(A) SUM $= A \cdot B + \overline{A}\,\overline{B}$
(B) SUM $= A \cdot \overline{B} + \overline{A} \cdot B$
(C) CARRY $= A \cdot B$
(D) CARRY $= A + B$

Which is these expressions are correct ?

(A) 1 and 3 (B) 2 and 3

(C) 2 and 4 (D) 1 and 4

MCQ 83

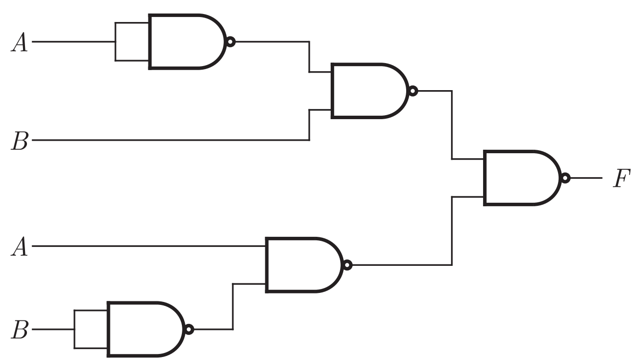
For a binary half-subtractor having two inputs A and B, the correct sets of logical expressions for the output D (= A minus B) and X (= borrow) are

(A) $D = AB + \overline{A}B,\ X = \overline{A}B$ (B) $D = \overline{A}B + A\overline{B},\ X = A\overline{B}$

(C) $D = \overline{A}B + A\overline{B},\ X = \overline{A}B$ (D) $D = AB + \overline{A}\,\overline{B},\ X = A\overline{B}$

MCQ 84

The circuit shown below is functionally equivalent to



(A) NOR gate (B) OR gate

(C) Ex-OR gate (D) NAND gate

MCQ 85

Match **List - I** (Digital Circuit) with **List - II** (Circuit Type) and select the correct answer using the codes given below the lists :

	List - I		List - II
a.	BCD to 7-segment	**1.**	Sequential circuit decoder
b.	4-to-1 multiplexer	**2.**	Combinational circuit
c.	4-bit shift register	**3.**	Neither sequential nor combinational circuit
d.	BCD counter		

Codes :

	a	b	c	d
(A)	2	1	2	1
(B)	3	2	1	3
(C)	2	2	1	1
(D)	3	1	2	3

MCQ 86

The output of a Moore sequential machine is a function of

(A) All present states of the machine

(B) All the inputs

(C) A few combination of inputs and the present state

(D) All the combination of inputs and the present state

MCQ 87

Minimum number of *J-K* flip-flops needed to construct a BCD counter is

(A) 2 (B) 3

(C) 4 (D) 5

MCQ 88

A 10 bit ADC with full scale output voltage of 10.24 V is designed to have a $\pm$ LSB/2 accuracy. If the ADC is calibrated at 25°C and the operating temperature ranges from 0°C to 50°C, then the maximum net temperature coefficient of ADC should not exceed

(A) $\pm 200\,\mu V/^\circ C$ (B) $\pm 400\,\mu V/^\circ C$

(C) $\pm 600\,\mu V/^\circ C$ (D) $\pm 800\,\mu V/^\circ C$

MCQ 89

The characteristic equation for the next state (Q_{n+1}) of a *J-K* flip-flop is

(A) $(Q_{n+1}) = JQ_n + K\overline{Q}_n$ (B) $Q_{n+1} = \overline{J}\,\overline{Q}_n + \overline{K}\,\overline{Q}_n$

(C) $Q_{n+1} = J\overline{Q}_n + \overline{K}Q_n$ (D) $Q_{n+1} = JQ_n + KQ_n$

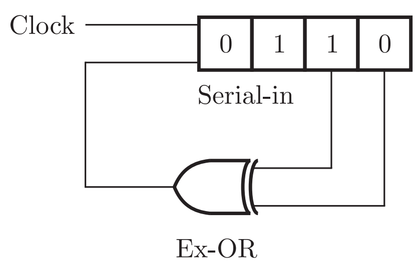
MCQ 90

The number of unused states in a 4-bit Johnson counter is

(A) 2
(B) 4
(C) 8
(D) 12

MCQ 91

The initial contents of the 4-bit series-in-parallel-out, right shift, shift register as shown are 0110. After 3 clock pulses the contents of the shift register will be



(A) 0000
(B) 0101
(C) 1010
(D) 1110

MCQ 92

Assertion (A) : The switching speed of ECL gate is very high.

Reason (R) : The devices in ECL gate operate in active region.

(A) Both A & R are true and R is the correct explanation of A
(B) Both A & R are true but R is NOT the correct explanation of A
(C) A is true but R is false
(D) A is false but R is true

MCQ 93

Assertion (A) : When transistor switches are to be used in an application where speed is a premium, it is better to reduce the storage time.

Reason (R) ; It is comparatively easy to reduce storage time rather than the rise time and fall time of a transistor switch.

(A) Both A & R are true and R is the correct explanation of A
(B) Both A & R are true but R is NOT the correct explanation of A

(C) A is true but R is false

(D) A is false but R is true

MCQ 94

Assertion (A) : Asynchronous sequential circuits are difficult to design.

Reason (R) : External clock is used for synchronization of asynchronous sequential circuits.

(A) Both A & R are true and R is the correct explanation of A

(B) Both A & R are true but R is NOT the correct explanation of A

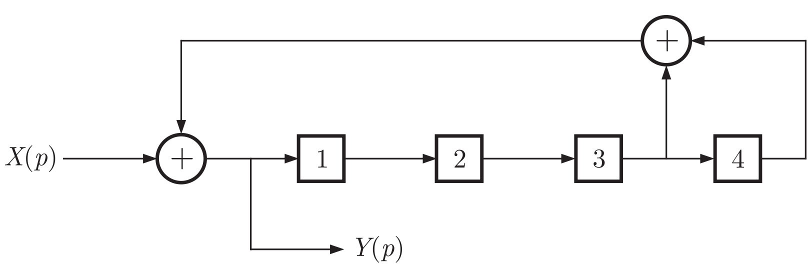
(C) A is true but R is false

(D) A is false but R is true

YEAR 2004

MCQ 95

Consider the following circuits of a scrambler :



$X(p) \triangleq$ shift data system polynomial

$Y(p) \triangleq$ output data stream polynomial

$\square$'s $\triangleq$ shift-register stages

$\oplus$'s $\triangleq$ XOR gates

Which one of the following relates $X(p)$ and $Y(p)$?

(A) $Y(p) = X(p)/[p^4 + p^3 + 1]$

(B) $Y(p) = p^4 X(p)/[p^4 + p^3 + 1]$

(C) $Y(p) = X(p)/[p^4 + p + 1]$

(D) $Y(p) = p^4 X(p)/[p^4 + p + 1]$

MCQ 96

How many 1's are present in the binary representation of $(4 \times 4096) + (9 \times 256) + (7 \times 16) + 5$?

(A) 8 (B) 9

(C) 10 (D) 11

MCQ 97

Assume that only x and y logic inputs are available, and their complements $\overline{x}$ and $\overline{y}$ are not available. What is the minimum number of 2-input NAND gates required to implement $x \oplus y$?

(A) 2 (B) 3

(C) 4 (D) 5

MCQ 98

A, B and C are three boolean variables. Which one of the following boolean expressions cannot be minimized any further ?

(A) $Z = A\overline{B}\,\overline{C} + AB\overline{C} + ABC + \overline{A}\,\overline{B}\,\overline{C}$

(B) $Z = A\overline{B}C + AB\overline{C} + ABC + \overline{A}\,\overline{B}\,\overline{C}$

(C) $Z = A\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,C + ABC + \overline{A}\,B\,\overline{C}$

(D) $Z = \overline{A}\,B\overline{C} + AB\overline{C} + ABC + \overline{A}\,\overline{B}C$

MCQ 99

What is the minimum number of NAND gates required to implement $A + A\overline{B} + A\overline{B}C$?

(A) 0 (B) 1

(C) 4 (D) 7

MCQ 100

Match **List - I** (Logic gates) with **List - II** (Characteristics) and select the correct answer using the codes :

	List - I		List - II
a.	HTL	**1.**	High fan-out
b.	CMOS	**2.**	Highest speed of operation
c.	I^2L	**3.**	Highest noise immunity

d. ECL **4.** Lowest product of power and delay

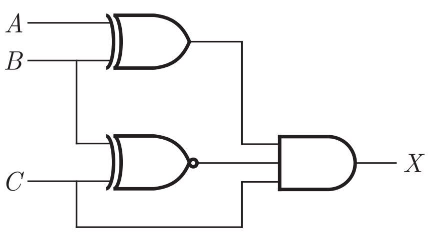
Codes :

	a	b	c	d
(A)	3	2	4	1
(B)	4	2	3	1
(C)	3	1	4	2
(D)	4	1	3	2

MCQ 101

Consider the following logic circuit :

What is the required input condition (A, B, C) to make the output $X = 1$, for the above logic circuit ?



(A) (1, 0, 1) (B) (0, 0, 1)

(C) (1, 1, 1) (D) (0, 1, 1)

MCQ 102

The output of a two level AND-OR gate network is F. What is the output when all the gates are replaced by NOR gates ?

(A) F (B) $\overline{F}$

(C) F^D (D) $\overline{F}^D$

where F^D is the dual function of F

MCQ 103

Which one of the following statements is correct ?

(A) PROM contains a programmable 'AND' array and a fixed 'OR' array.

(B) PLA contains a fixed 'AND' array and a programmable 'OR' array.

(C) PROM contains a fixed 'AND' array and a programmable 'OR' array.

(D) PLA contains a programmable 'AND' array and a programmable 'NOR' array.

MCQ 104

Which one of the following statements describes the operation of a multiplexer ?

(A) A logic circuit used to generate coded output.

(B) A logic circuit used to generate F's complement.

(C) A logic circuit that accepts two or more inputs and allows one of them at a time to get through the output.

(D) A logic circuit that transmits one input to several output lines.

MCQ 105

A ROM is to be used to implement a " squarer", which outputs the square of a 4-bit number. What must be the size of the ROM ?

(A) 16 address lines and 16 data lines

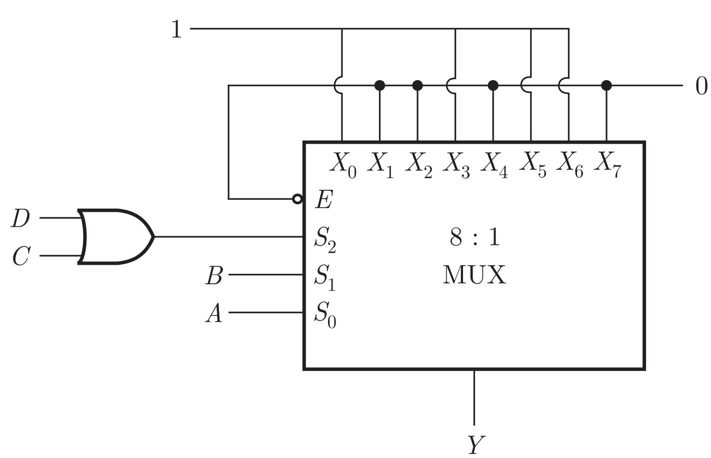
(B) 4 address lines and 8 data lines

(C) 8 address lines and 8 data lines

(D) 4 address lines and 16 data lines

MCQ 106

Consider the following circuit :



In the above TTL circuit, S_2 to S_0 are select lines and X_7 to X_0 are input lines. S_0 and X_0 are LSBs. What is the output Y ?

(A) Indeterminable
(B) $A \oplus B$
(C) $\overline{A \oplus B}$
(D) $\overline{C \oplus B \oplus A}$

MCQ 107

Which one of the following statements is not correct ?

(A) An 8-input MUX can be used to implement any 4 variable function.
(B) A 3-lines-to-8-lines DEMUX can be used to implement any 4 variable function.
(C) A 64-input MUX can be build using nine 8 input MUXs.
(D) A 6-lines-to-64-lines DEMUX can be built using nine 3-lines-to-8-lines DEMUXs.

MCQ 108

Consider the following statements :

For a master-slave J-K flip-flop,

1. The toggle frequency is the maximum clock frequency at which the flip-flop will toggle reliably.
2. The data input must [recede the clock triggering edge transition time by some minimum time.
3. The data input must remain fixed for a given time after the clock triggering edge transition time for reliable operation.
4. Propagation delay time is equal to the rise time and fall time of the data.

Which of the statements given below are correct ?

(A) 1, 2 and 3
(B) 1, 2 and 4
(C) 1, 3 and 4
(D) 2, 3 and 4

MCQ 109

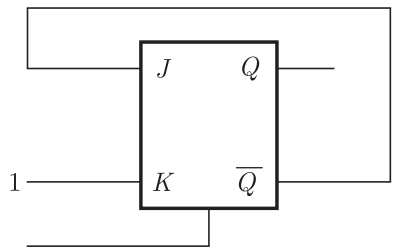
The total number of 1's in a 15-bit shift register is to be counted by clocking into a counter which is preset to 0. The counter must have which one of the following ?

(A) 4-bits
(B) 5-bits

(C) 16-bit (D) 6-bits

MCQ 110

Consider the following J-K flip-flop :



In the above J-K flip-flop, $J = \overline{Q}$ and $K = 1$. Assume that the flip-flop was initially cleared and then clocked for 6 pulses.

What is the sequence at the Q output ?

(A) 01000 (B) 011001

(C) 010010 (D) 010101

MCQ 111

Consider the following statements regarding registers and latches :

1. Registers are made of edge-triggered FFs, whereas latches are made from level-triggered FFs.
2. Register are temporary storage devices whereas latches are not.
3. A latch employs cross-coupled feedback connections.
4. A register stores a binary word whereas a latch does not.

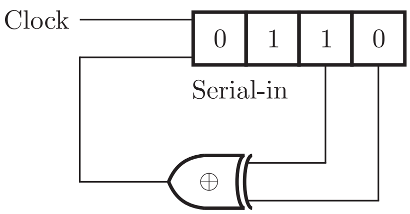
Which of the statements given above are correct ?

(A) 1 and 2 (B) 1 and 3

(C) 2 and 3 (D) 3 and 4

MCQ 112

Consider the following shift right register :



The initial contents of the 4-bit serial-in-parallel-out, shift right register shown above are 0110. What will be the contents of the register after 3 clock pulses are required ?

(A) 0000 (B) 0101

(C) 1010 (D) 1111

MCQ 113

Match **List - I** (Type of *N*-bit ADC) with **List - II** (Characteristics) and select the correct answer using the codes given below the lists :

	List - I		List - II
a.	Flash	**1.**	Integrating type
b.	Successive	**2.**	Fastest converter
c.	Counter ramp	**3.**	Maximum conversion time $= N$ bits
d.	Dual slope	**4.**	Uses a DAC in its feedback path

Codes :

	a	b	c	d
(A)	1	4	3	2
(B)	1	3	4	2
(C)	2	4	3	1
(D)	2	3	4	1

YEAR 2005

MCQ 114

Match **List - I** (Programmable Logic Device) with **List - II** (Function) and select the correct answer using the codes given below the lists :

List - I **List - II**

a.	EPROM	**1.**	AND-gate programmable, OR-gate permanently hardwired
b.	PLA	**2.**	Both AND and OR-gates
c.	GAL	**3.**	AND-gate programmable, OUTPUT permanently hardwired but may be taken through resistor, or tristate gate programmable
d.	PAL	**4.**	AND-gate permanently hardwired, OR-gate programmable

Codes :

	a	b	c	d
(A)	4	1	3	2
(B)	3	2	4	1
(C)	4	2	3	1
(D)	3	1	4	2

MCQ 115

Consider the following statements :

1. MOSFET ROMs have much larger capacities than those of the BJT ROMs.
2. BJT ROMs are faster that the MOSFET ROMs.
3. BJT RAM memories can be static or dynamic.

Which of the statements given above is/are correct ?

(A) 1 only　　(B) 1 and 2

(C) 2 and 3　　(D) 1, 2 and 3

MCQ 116

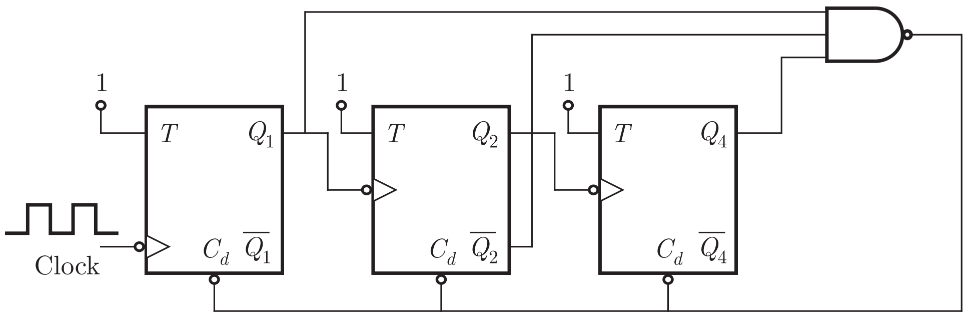
12 MHz clock frequency is applied to a cascaded counter of modulus-3 counter, modulus-4 counter and modulus-5 counter. What are the lowest output frequency and the overall modulus, respectively ?

(A) 200 kHz, 60　　(B) 1 MHZ, 60

(B) 3 MHz, 12　　(D) 4 MHz, 12

MCQ 117

The circuit given above is that of a



(A) Mod-5 counter
(B) Mod-6 counter
(C) Mod-7 counter
(D) Mod-8 counter

MCQ 118

A 1-bit full-adder takes 20 ns to generate carry-out bit and 40 ns for the sum bit. What is the maximum rate of addition per second when four 1-bit full-adders are cascade ?

(A) 10^7
(B) 1.25×10^7
(C) 6.25×10^6
(D) 10^5

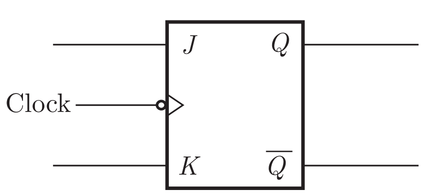
MCQ 119

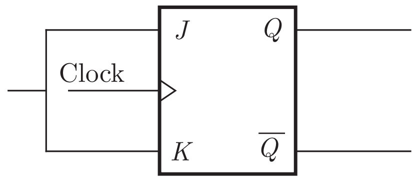
Match **List - I** (Type of flip-flop) with **List - II** (Symbol) and select the correct answer using the code given below the lists :

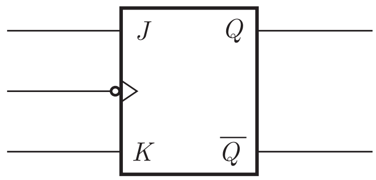
List - I

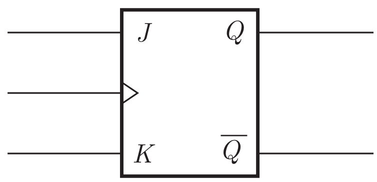
a. T flip-flop
b. Level-triggered J-K flip-flop
c. Leading edge-triggered J-K flip-flop
d. Trailing edge-triggered J-K flip-flop

List - II

1. 

2. 

3. 

4. 

Codes :

	a	b	c	d
(A)	1	2	3	4
(B)	2	1	3	4
(C)	1	2	4	3
(D)	2	1	4	3

MCQ 120

If $(2.3)_{\text{base } 4} + (1.2)_{\text{base } 4} = (y)_{\text{base } 4}$; what is the value of y ?

(A) 10.1 (B) 10.01

(C) 10.2 (D) 1.02

MCQ 121

The number of 1 in 8-bit representation of -127 in 2's complement form is m and that in 1's complement form is n. What is the value of $m:n$?

(A) 2 : 1 (B) 1 : 2

(C) 3 : 1 (D) 1 : 3

MCQ 122

Given $(135)_{\text{base } x} + (144)_{\text{base } x} = (323)_{\text{base } x}$

What is the value of base x ?

(A) 5
(B) 3
(C) 12
(D) 6

MCQ 123

Assertion (A) : The speed power product is an important parameter for comparing various TTL series.

Reason (R) : A low value of speed power product indicates that a propagation delay can be achieved without excessive power dissipation and vice-versa.

(A) Both A & R are true and R is the correct explanation of A
(B) Both A & R are true but R is NOT the correct explanation of A
(C) A is true but R is false
(D) A is false but R is true

MCQ 124

Consider the following statements :

A 4 : 16 decoder can be constructed (with enable) by :

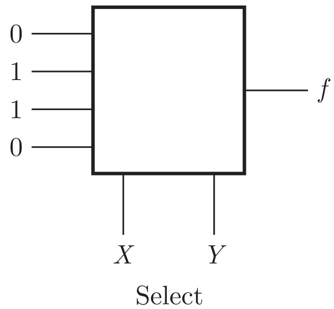
1. Using four 2 : 4 decoder (each with an enable input) only.
2. Using five 2 : 4 decoders (each with an enable input) only.
3. Using two 3 : 8 decoders (each with an enable input) only.
4. Using two 3 : 8 decoders (each with an enable input) and an inverter.

Which of the statements given above is/are correct.

(A) 2 and 3
(B) 1 only
(C) 2 and 4
(D) None of the above

MCQ 125

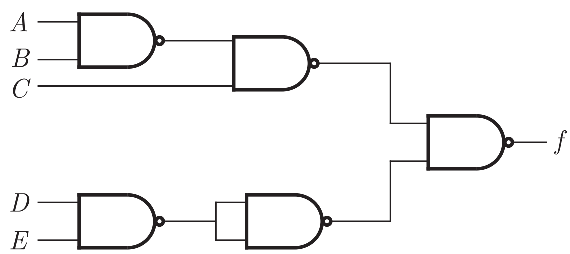
What is the output $f(x, y)$ of the multiplexer resulting from the input logical values ?



(A) An Ex-OR gate
(B) A NOR gate
(C) An AND gate
(D) A NAND gate

MCQ 126

Which one of the following functions is realized by the circuits shown below ?



(A) $(\overline{A}+\overline{B})\,C+\overline{DE}$
(B) $(A+B)\,C+D+E$
(C) $AB+C+DE$
(D) $AB+C(D+E)$

MCQ 127

Which one of the following statements is not correct ?

(A) A full adder can be constructed using two half-adders and an OR gate.
(B) Two four bit parallel adders can be cascaded to construct 8-bit parallel adder.
(C) Ripple carry adder has addition time independent of the number of bits.
(D) Carry look-ahead is used to speed up the parallel addition.

MCQ 128

Consider the following statements :

A half-adder

1. Is a half-subtractor also.
2. Has two outputs $C_H = x.y$ and $S_H = x \oplus y$ for two input x and y.
3. Has two outputs $C_H = x + y$ and $S_H = x \oplus y$ for two inputs x and y.
4. Is a combinational circuit.

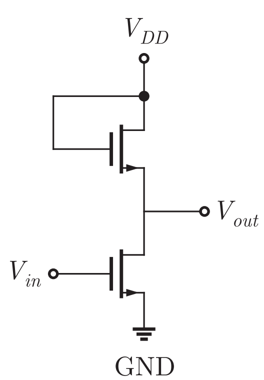
Which of the statements given above is/are correct ?

(A) 1, 3 and 4 (B) 1, 2, and 4

(C) 4 only (D) 2 and 3

MCQ 129

In the circuit given below, both transistors have the same V_T. What is the approximate value of the highest possible output voltage V_{out}, if V_{in} can range from 0 to V_{DD} ? (Assume $0 < V_T < V_{DD}$)



(A) $V_{DD} - V_T$ (B) V_{DD}

(C) V_T (D) 0

MCQ 130

What is the minimized logic expression corresponding to the given karnaugh map ?

$wx \backslash yz$	00	01	11	10
00			1	
01	1	1	1	
11		1	1	1
10		1		

(A) xz

(B) $\overline{w}x\overline{y} + \overline{w}yz + w\overline{y}z + wxy$

(C) $\overline{w}x\overline{y} + \overline{w}yz + w\overline{y}\,\overline{z} + wx\overline{y}$

(D) $xz + \overline{w}yz + \overline{w}x\overline{y} + wxy + w\overline{y}z$

MCQ 131

The boolean function $(x+y)(\overline{x}+z)(y+z)$ is equal to which one the following expressions ?

(A) $(x+y)(y+z)$

(B) $(\overline{x}+z)(y+z)$

(C) $(x+y)(\overline{x}+z)$

(D) $(x+y)(x+\overline{z})$

MCQ 132

$AB+\overline{A}C=(A+C)(\overline{A}+B)$........

Which one of the following is the dual form of the boolean identity given above ?

(A) $AB+\overline{A}C=AC+\overline{A}B$

(B) $(A+B)(\overline{A}+C)=(A+C)(\overline{A}+B)$

(C) $(A+B)(\overline{A}+C)=AC+\overline{A}B$

(D) $AB+\overline{A}C=AB+\overline{A}C+BC$

MCQ 133

A gray code is a/an :

(A) Binary weight code

(B) Arithmetic code

(C) Code which exhibits a single bit change between two successive codes

(D) Alphanumeric code

YEAR 2006

MCQ 134

Consider the following statements describing the property of a complementary MOS (CMOS) inverter :

1. It is combination of an n-channel FET and a p-channel FET.
2. There is power dissipation when the input carries the logical 1 signal.
3. There is no power dissipation when the input carries the logical 1 signal.
4. There is power dissipation during transition from 0 to 1 or from 1 to 0.

Which of the statements given above are correct ?

(A) 1, 2 and 3
(B) 2, 3 and 4
(C) 1, 3 and 4
(D) 1, 2 and 4

MCQ 135

A single ROM is used to design a combinational circuit described by a truth-table. What is the number of address lines in the ROM ?

(A) Number of input variables in the truth table
(B) Number of output variables in the truth-table
(C) Number of input plus output variables in the truth-table
(D) Number of lines in the truth-table

MCQ 136

Which one of the following equations satisfies the J-K flip-flop truth tables ?

(A) $Q_{n+1} = J_n \overline{Q}_n + \overline{K}_n Q_n$
(B) $Q_{n+1} = \overline{J}_n \overline{Q}_n + \overline{K}_n Q_n$
(C) $Q_{n+1} = J_n Q_n + K_n Q_n$
(D) $Q_{n+1} = \overline{J}_n \overline{Q}_n + \overline{K}_n \overline{Q}_n$

MCQ 137

What is the number of selector lines required in a single input n -output demultiplexer ?

(A) 2
(B) n
(C) 2^n
(D) $\log_2 n$

MCQ 138

A master-slave configuration consists of two identical flip-flops connected in such a way that the output of the master is input to the slave. Which one of the following is correct ?

(A) Master is level triggered and slave is edge triggered

(B) Master is edge triggered and slave is level triggered

(C) Master is positive edge triggered and slave is negative edge triggered.

(D) Master is negative edge triggered and slave is positive edge triggered

MCQ 139

Match **List - I** (Circuit) with **List - II** (Application) and select the correct answer using the code given below the lists :

	List - I		List - II
a.	Ripple up counter	**1.**	Division
b.	Synchronous down counter	**2.**	Multiplication
c.	Shift left register	**3.**	To create delay
d.	Shift right register	**4.**	Transient states

Codes :

	a	b	c	d
(A)	2	3	4	1
(B)	4	1	2	3
(C)	2	1	4	3
(D)	4	3	2	1

MCQ 140

Which one of the following D/A converters has the resolution of approximately 0.4 % of its full scale range ?

(A) 8-bit

(B) 10-bit

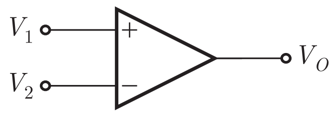
(C) 12-bit

(D) 16-bit

MCQ 141

How can the voltage comparator shown in the circuit given below be

used in the analog-to-digital conversion ?



(A) As a 1-bit quantizer
(B) As a 2-bit quantizer
(C) As a 4-bit quantizer
(D) As a 8-bit quantizer

MCQ 142

A 10-bit A/D converter is used to digitize an analog signal in the 0 to 5 V range. What is the approximate value of the maximum peak to peak ripple voltage that can be allowed in the d.c supply voltage ?

(A) 100 mV
(B) 50 mV
(C) 25 mV
(D) 5.0 mV

MCQ 143

Given below are three types of converters :

1. Successive approximation type
2. Weighted-resistor type
3. R-2R ladder type

Which of these types are D to A converters ?

(A) Only 1 and 2
(B) Only 2 and 3
(C) Only 1 and 3
(D) 1, 2 and 3

MCQ 144

What is the gray code word for the binary 101011 ?

(A) 101011
(B) 110101
(C) 011111
(D) 111110

MCQ 145

Which of the following subtraction operations results in F_{16} ?

1. $(BA)_{16} - (AB)_{16}$
2. $(BC)_{16} - (CB)_{16}$
3. $(CB)_{16} - (BC)_{16}$

Select the correct answer using the code given below :

(A) Only 1 and 2
(B) Only 1 and 3
(C) Only 1 and 3
(D) 1, 2 and 3

MCQ 146

Assertion (A) : To obtain high switching speed in BJT based logic circuits, transistors are operated in active region.

Reason (R) : In active region, a transistor works as a linear element.

(A) Both A & R are true and R is the correct explanation of A
(B) Both A & R are true but R is NOT the correct explanation of A
(C) A is true but R is false
(D) A is false but R is true

MCQ 147

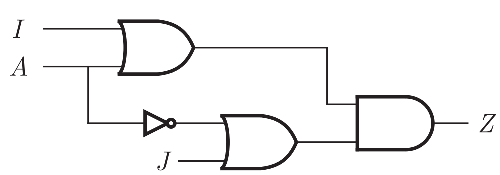
The boolean expression $Y(A,B,C) = A + BC$ is to be realized using 2-input gates of only one type. What is the minimum number of gates required for the realization ?

(A) 1
(B) 2
(C) 3
(D) 4 or more

MCQ 148

$I = 1, \quad J = B$

The circuit shown is to be used to implement the function $Z = f(A,B) = \overline{A} + B$



What values are to be selected for I and J ?

(A) $I = 0, \quad J = B$
(B) $I = A, \quad J = B$
(B) $I = B, \quad J = 1$
(D) $I = \overline{B}, \quad J = 0$

MCQ 149

The boolean expression $X(P,Q,R) = \pi(0,5)$ is to be realized using

only two 2-input gates. Which are these gates ?

(A) AND and OR (B) NAND or OR

(C) AND and Ex-OR (D) OR and Ex-OR

MCQ 150

Match **List - I** (Logic gate) with **List - II** (Characteristic) and select the correct answer using the code given below the lists :

	List - I		List - II
a.	HTL	**1.**	High fan-out
b.	CMOS	**2.**	Highest speed of operation
c.	I^2L	**3.**	High noise immunity
d.	ECL	**4.**	Lowest product of power and delay

Codes :

	a	b	c	d
(A)	3	4	1	2
(B)	2	1	4	3
(C)	3	1	4	2
(D)	2	4	1	3

MCQ 151

Match **List - I** (TTL Nos.) with **List - II** (Significance) and select the correct answer using the code given below the lists :

	List - I		List - II
a.	74 LS 00	**1.**	Lowest power/low speed
b.	74 H 00	**2.**	High speed/high power
c.	74 00	**3.**	Basic NAND gate
d.	74 L 00	**4.**	Low power schottky

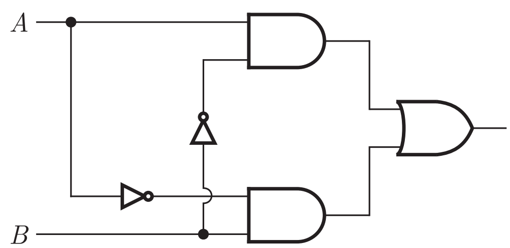
Codes :

	a	b	c	d
(A)	4	2	3	1
(B)	3	1	4	2
(C)	4	1	3	2

(D) 3 2 4 1

MCQ 152

Which one of the following logical operations is performed by the digital circuit shown below ?



(A) NOR (B) NAND

(C) Ex-OR (D) OR

MCQ 153

What is the boolean expression for the truth table shown below ?

A	0	0	0	0	1	1	1	1
B	0	0	1	1	0	0	1	1
C	0	1	0	1	0	1	0	1
f	0	0	0	1	0	0	1	0

(A) $B(A+C)(\overline{A}+\overline{C})$ (B) $B(A+\overline{C})(\overline{A}+C)$

(C) $\overline{B}(A+C)(\overline{A}+C)$ (D) $\overline{B}(A+C)(\overline{A}+\overline{C})$

MCQ 154

What does the boolean expression

$AD+ABCD+ACD+\overline{A}B+ACD+\overline{A}\,\overline{B}$

on minimization result into ?

(A) $A+D$ (B) $AD+\overline{A}$

(C) AD (D) $\overline{A}+D$

MCQ 155

If A and B are boolean variables, then what is $(A+B)\cdot(A+\overline{B})$

(A) B (B) A

(C) $A+B$ (D) AB

MCQ 156

What is the boolean expression $A \oplus B$ equivalent to ?

(A) $AB+\overline{A}\,\overline{B}$ (B) $\overline{A}B+A\overline{B}$

(C) B (D) $\overline{A}$

YEAR 2007

MCQ 157

When two 16-input multiplexers drive a 2-input MUX, what is the result ?

(A) 2-input MUX (B) 4-input MUX

(C) 16-input MUX (D) 32-input MUX

MCQ 158

The characteristic equation of a flip-flop gives the next state Q_{N+1} in terms of the present state Q_N and the inputs. Which one of the following is the characteristic equation of J-K flip-flop ?

(A) $Q_{N+1}=J\overline{Q}_N+\overline{K}Q_N$ (B) $Q_{N+1}=J+\overline{K}Q_N$

(C) $Q_{N+1}=K\overline{Q}_N+\overline{J}Q_N$ (D) $Q_{N+1}=K+\overline{J}Q_N$

MCQ 159

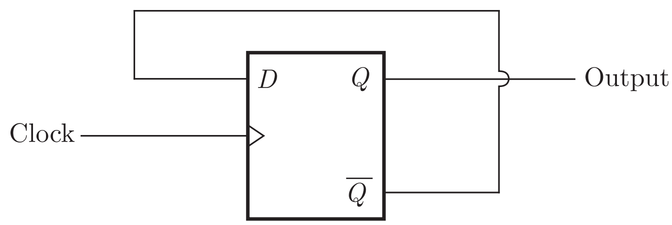
A 1 ms pulse can be converted into a 10 ms pulse bu using which one of the following ?

(A) An astable multivibrator (B) A monostable multivibrtor

(C) A bistable multivibrator (D) A J-K flip-flop

MCQ 160

For the circuit shown in the figure, what is the frequency of the output Q ?



(A) Twice the input clock frequency

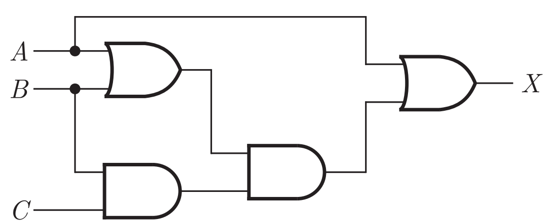
(B) Half the input clock frequency

(C) Same as the input clock frequency

(D) Inverse of the propagation delay of the FF

MCQ 161

For the logic circuit given above, what is the simplified boolean function ?



(A) $X = AB + C$

(B) $X = BC + A$

(C) $X = AB + AC$

(D) $X = AC + B$

MCQ 162

The product of which of the following gives the figure of merit of a logic family ?

(A) Gain and bandwidth

(B) Propagation delay time and power dissipation

(C) Fan-out and propagation delay time

(D) Noise margin and power dissipation

MCQ 163

Assume that only x and y logic inputs are available, and their complements $\overline{x}$ and $\overline{y}$ are not available. What is the minimum number of 2-input of NAND gates required to implement $x \oplus y$?

(A) 2

(B) 3

(C) 4 (D) 5

MCQ 164

Which one of the following is the correct sequence of the numbers represented in the series given below ?

$(2)_3$, $(10)_4$, $(11)_5$, $(14)_6$, $(22)_7$, ...

(A) 2, 3, 4, 5, 6, ... (B) 2, 4, 6, 8, 10,........

(C) 2, 4, 6, 10, 12,......... (D) 2, 4, 6, 10, 16,.......

MCQ 165

What is the addition of $(-64)_{10}$ and $(80)_{16}$?

(A) $(-16)_{10}$ (B) $(16)_{16}$

(C) $(1100000)_2$ (D) $(01000000)_2$

MCQ 166

When the boolean function $F(x_1, x_2, x_3) = \Sigma(0,1,2,3) + \Sigma_\Phi(4,5,6,7)$ is minimized, what does one get ?

(A) 1 (B) 0

(C) x_1 (D) x_3

MCQ 167

Consider the following statements :

For 3 input variables a, b, c; a boolean function $y = ab + bc + ca$ represents

1. A 3-input majority gate.
2. A 3-input minority gate.
3. Carry output of a full adder.
4. Product circuit for a, b and c.

Which of the above statements are correct ?

(A) 1 and 4 only (B) 2 and 3 only

(C) 1 and 3 only (D) 3 and 4 only

MCQ 168

By inspecting the K-map plot of the switching function

$F(x_1, x_2, x_3) = \Sigma(1, 3, 6, 7)$ one can say that the redundant prime implicant is

(A) $\overline{x}_1 x_3$ (B) $x_2 x_3$

(C) $x_1 x_2$ (D) x_3

MCQ 169

Match **List - I** (Boolean logic function) with **List - II** (Inverse of function) and select the correct answer using the code given below the lists :

	List - I		**List - II**
a.	$ab + bc + ca + abc$	**1.**	$\overline{a}(\overline{b} + \overline{c})$
b.	$ab + \overline{a}\,\overline{b} + \overline{c}$	**2.**	$\overline{a}\,\overline{b} + \overline{b}\,\overline{c} + \overline{c}\,\overline{a}$
c.	$a + bc$	**3.**	$(a \oplus b)\,c$
d.	$(\overline{a} + \overline{b} + \overline{c})(a + \overline{b} + \overline{c})(\overline{a} + \overline{b} + c)$	**4.**	$abc + \overline{a}bc + ab\overline{c}$

Codes :

	a	b	c	d
(A)	3	2	1	4
(B)	2	3	1	4
(C)	3	2	4	1
(D)	2	3	4	1

MCQ 170

Why does an I^2L (Integrated Injection Logic) have higher density of integration than TTL ?

(A) It does not require transistors with high current gain and hence they have smaller geometry

(B) It uses multicollector transistors

(C) It does not require isolation diffusion

(D) It uses dynamic logic instead of static logic

MCQ 171

Consider the following statements :

1. Minimization using karnaugh map may not provide unique solution.
2. Redundant grouping in karnaugh map may result in non-minimized solution.
3. Don't care states if used in karnaugh map for minimization, the minimal solution is not obtained.

Which of the statements given above are correct ?

(A) 1, 2 and 3 (B) 2 and 3 only

(C) 1 and 3 only (D) 1 and 2 only

MCQ 172

Match **List - I** (Logic gates) with **List - II** (Characteristics) and select the correct answer using the codes given below the lists :

	List - I		List - II
a.	HTL	**1.**	High fan-out
b.	CMOS	**2.**	Highest speed of operation
c.	I^2L	**3.**	High noise immunity
d.	ECL	**4.**	Lowest product of power and delay

Codes :

	a	b	c	d
(A)	3	2	4	1
(B)	4	2	3	1
(C)	3	1	4	2
(D)	4	1	3	2

MCQ 173

Consider the following statements :

1. CMOS gates require very little power when they are not changing states.
2. Transmission gates are widely used in CMOS designs.
3. CMOS circuit have considerable resistance to noise.

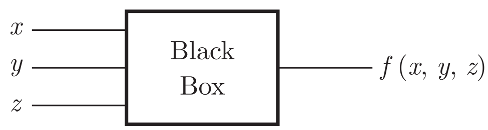
Which of the statements given above are correct ?

(A) 1 and 2 only (B) 2 and 3 only
(C) 1 and 3 only (D) 1, 2 and 3

MCQ 174

The black box in the figure consists of a minimum complexity circuit that uses only AND, OR and NOT gates.

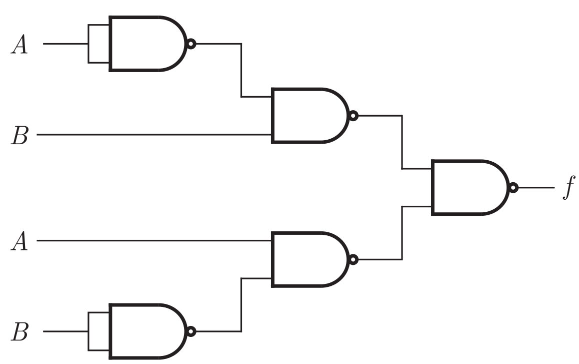
The function $f(x, y, z) = 1$ whenever x, y are different and 0 otherwise. In addition the 3 inputs x, y, z are never all the same value. Which one of the following equations leads to the correct design for the minimum complexity circuit ?



(A) $x'y + xy'$ (B) $x + y'z$
(C) $x'y'z' + xy'z$ (D) $xy + y'z + z'$

MCQ 175

The circuit shown below is functionally equivalent to which one of the following ?



(A) NOR gate (B) OR gate
(C) Ex-OR gate (D) NAND gate

MCQ 176

Which one of the following statements is correct ?

(A) Static-1 hazard may occur in a 2-level AND-OR gate network.

(B) Static-0 hazard may occur may occur in a 2-level AND-OR gate network.

(C) Dynamic hazard may occur in a 2-level OR-AND gate network.

(D) Essential hazards may occur in a combinational logic circuit.

YEAR 2008

MCQ 177

In order to build a 3-bit simultaneous A/D converter, what is the number of comparators required in circuit ?

(A) 7
(B) 8
(C) 15
(D) 16

MCQ 178

The boolean functions can be expressed in canonical SOP (Sum Of Products) and POS (Product Of Sums) form. For the functions, $Y = A + \overline{B}C$, which are such two forms

(A) $Y = \Sigma(1,2,6,7)$ and $Y = \Pi(0,2,4)$

(B) $Y = \Sigma(1,4,5,6\,7)$ and $Y = \Pi(0,2,3)$

(C) $Y = \Sigma(1,2,5,6,7)$ and $Y = \Pi(0,1,3)$

(D) $Y = \Sigma(1,2,4,5,6,7)$ and $Y = \Pi(0,2,3,4)$

MCQ 179

The boolean function $A + BC$ is a reduced form of which one of the following

(A) $AB + BC$
(B) $\overline{A}B + A\overline{B}C$
(C) $(A + B)\cdot(A + C)$
(D) None of the above

MCQ 180

Which one of the following statements is not correct ?

(A) $X + \overline{X}Y = X$
(B) $X(\overline{X} + Y) = XY$
(C) $XY + X\overline{Y} = X$
(D) $ZX + Z\overline{X}Y = ZX + ZY$

MCQ 181

A discrete source produces 8 symbols and is memoryless. Its entropy

is

(A) 1 bit/symbol only (B) 2 bits/symbol only

(C) 3 bits/symbol only (D) $\leqslant 3$ bits/symbol only

MCQ 182

$(24)_8$ is expressed in gray code as which one of the following ?

(A) 11000 (B) 10100

(C) 11110 (D) 11111

MCQ 183

Assertion (A) : *D* flip-flops are used as buffer register.

Reason (R) : Flip-flops are free from "race-around" condition.

(A) Both A & R are true and R is the correct explanation of A

(B) Both A & R are true but R is NOT the correct explanation of A

(C) A is true but R is false

(D) A is false but R is true

MCQ 184

The figure of merit of a logic family is given by

(A) Gain bandwidth product

(B) (Propagation delay time)×(Power dissipation)

(C) (Fan-out)×(Propagation delay time)

(D) (Noise margin)×(Power dissipation)

MCQ 185

The I^2L (Integrated Injection Logic) has higher density of integration the than TTL because it

(A) Does not required transistor with high current gain and hence they have smaller geometry

(B) Uses compact bipolar transistors

(C) Does not required isolation diffusion

(D) Uses dynamic logic instead of static logic

MCQ 186

Which one of the following statements is correct ?

(A) PROM contains a programmable AND array and a fixed OR array.

(B) PLA contains a fixed AND array and a programmable OR array.

(C) PROM contains a fixed AND array and a programmable OR array.

(C) PLA contains a programmable AND array and a fixed OR array.

MCQ 187

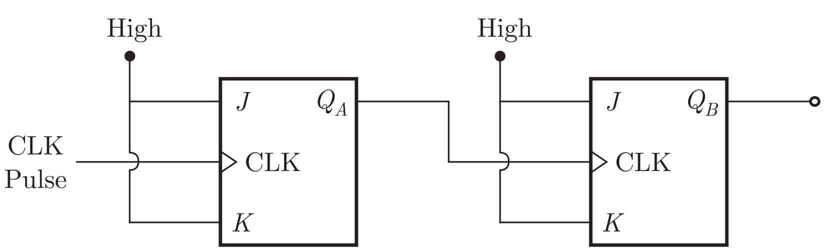
How many bits will a D/A converter uses so that its full scale output voltage is 5 V and its resolution is at the most 10 mV ?

(A) 5 (B) 7

(C) 9 (D) 11

MCQ 188

The below circuit illustrates a typical application of the *J*-*K* flip-flops. What does this represent ?



(A) A shift register (B) A data storage device

(C) A frequency divider circuit (D) A decoder circuit

MCQ 189

A digital multiplexer can be used for which of the following ?

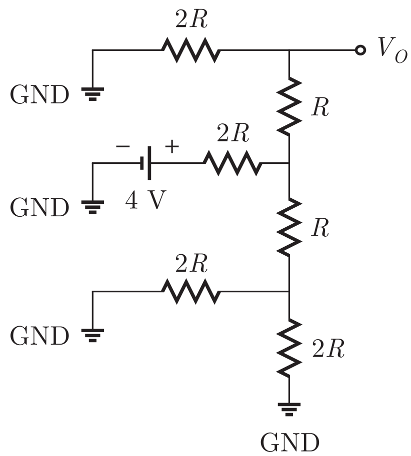
1. Parallel to serial conversion.
2. Many-to-one switch.
3. To generate memory chip select.
4. For code conversion.

Select the correct answer using the code given below :

(A) 1, 3 and 4
(B) 2, 3 and 4
(C) 1 and 2 only
(D) 2 and 3 only

MCQ 190

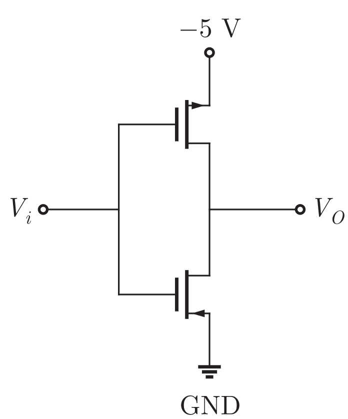
What is the output voltage 'V_O' of the $R - 2R$ decoder ladder network?



(A) 1 V
(B) 2 V
(C) 3 V
(D) 4 V

MCQ 191

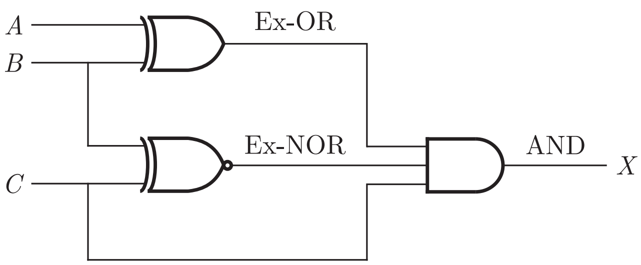
The threshold voltage for each transistor in the figure shown below is 2.0 V. What are the values of V_i for this circuit to work as an inverter ?



(A) -5 V and 0 V
(B) -5 V and 5 V
(C) 0 V and 5 V
(D) -3 V and 3 V

MCQ 192

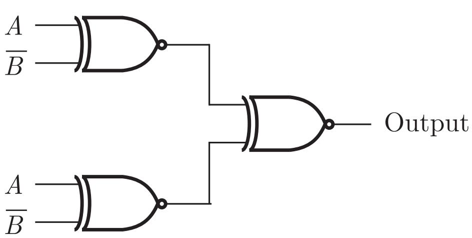
For the logic circuit shown in the figure, what is the required input condition (A, B, C) to make output $X = 1$?



(A) 1, 0, 1 (B) 0, 0, 1
(C) 1, 1, 1 (D) 0, 1, 1

MCQ 193

The output of the circuit shown in the figure is equal to



(A) 0 (B) 1
(C) $\overline{A}B + A\overline{B}$ (D) $(\overline{A \cdot B}) \cdot (\overline{A \cdot B})$

MCQ 194

Two 2's complement numbers having sign bits 'x' and 'y' are added and the sign bit of the result is 'z'. Which boolean function indicates the occurrence of the overflow ?

(A) xyz (B) $\overline{x}\,\overline{y}\,\overline{z}$
(C) $\overline{x}\,\overline{y}z + xy\overline{z}$ (D) $xy + yz + zx$

YEAR 2009

MCQ 195

Which of the following boolean algebra rules is correct ?

(A) $A \cdot \overline{A} = 1$ (B) $A + AB = A + B$
(C) $A + \overline{A}B = A + B$ (D) $A(A + B) = B$

MCQ 196

What are the ultimate purposes of minimizing logic expressions ?

1. To get a small size expression.
2. To reduce the number of variables in the given expression.
3. To implement the function of the logic expression with least hardware.
4. To reduce the expression for making it feasible for hardware implementation.

Select the correct answer from the codes given below :

(A) 1 only (B) 2 and 3
(C) 3 only (D) 3 and 4

MCQ 197

Which of the following factors are responsible to design IC logic gates to operate at a fixed supply voltage of 5 volts ?

1. Low heating of IC logic gates.
2. Compatibility with other logic gates.
3. Satisfactory and safe operation.
4. Standardization from IC manufacturing point of view.

Select the correct answer from the codes given below :

(A) 1 only (B) 2 only
(C) 2 and 3 (D) 3 and 4

MCQ 198

Which of the following statements is not correct ?

(A) Propagation delay is the time required for a gate to change its state.
(B) Noise immunity is the amount of noise which can be applied to the input of a gate without causing the gate to change state.
(C) Fan-in of a gate is always equal to fan-out of the same gate.
(D) Operating speed is the maximum frequency at which digital data can be applied to a gate.

MCQ 199

Which of the following are universal gates ?

1. NAND
2. NOR
3. Ex-OR

Select the correct answer from the codes given below :

(A) 1 and 2 only
(B) 1 and 3 only
(C) 2 and 3 only
(D)1, 2 and 3

MCQ 200

Which of the following output configurations are available in a TTL gate ?

1. Open collector output
2. Totem-pole output
3. Tri-state output

State the correct answer from the codes given below :

(A) 1 only
(B) 1 and 2 only
(C) 2 and 3 only
(D) 1, 2 and 3

MCQ 201

Which one of the following logic families can be operated using a supply voltage from 3 V to 15 V ?

(A) TTL
(B) ECL
(C) PMOS
(D) CMOS

MCQ 202

Which of the following circuits comes under the class of combinational logic circuits ?

1 Full-adder
2. Full-subtractor
3. Half-adder
4. *J-K* flip-flop
5. Counter

Select the correct answer from the codes given below :

(A) 1 only
(B) 3 and 4
(C) 4 and 5
(D) 1, 2 and 3

MCQ 203

Consider a multiplexer with X and Y as data inputs and Z as control input. $Z = 0$ selects input X and $Z = 1$ select the input. Y. What are the connections required to realize the 2-variable boolean function $f = T + R$, without using any additional hardware ?

(A) R to X, 1 to Y, T to Z
(B) T to X, R to Y, T to Z
(C) T to X, R to Y, 0 to Z
(D) R to X, 0 to Y, T to Z

MCQ 204

With which decoder it is possible to obtain many code conversions ?

(A) 2 line to 4 line
(B) 3 line to 8 line
(C) Not possible with any decoder
(D) 4 line to 16 line decoder

MCQ 205

Match **List - I** (Application of circuits) with **List - II** (Circuit Name) and select the correct answer using the code given below the lists :

	List - I		List - II
a	Divider	1.	Astable multivibrator
b	Clips input voltage at two predetermined levels	2.	Schmitt trigger
c	Square wave generator	3.	Bistable multivibrator
d	Narrow current pulse generator	4.	Blocking oscillator

Codes :

	a	b	c	d
(A)	4	2	1	3
(B)	3	2	1	4
(C)	4	1	2	3
(D)	3	1	2	4

MCQ 206

Consider the following statements :

For a master-slave J-K flip-flop,

1. The toggle frequency is the maximum clock frequency at which the flip-flop will toggle reliably.
2. The data input must precede the clock triggering edge transition time by some minimum time.
3. The data input must remain fixed for a given time after, the clock triggering edge transition time for reliable operation.
4. Propagation delay time is equal to the rise time and fall time of the data.

Which of the above statements is/are correct ?

(A) 1, 2 and 3 (B) 1 and 2 only
(C) 2 and 3 only (D) 3 and 4 only

MCQ 207

Consider the following statements :

1. A flip-flop is used to store 1-bit of information.
2. Race-around condition occurs in a J-K flip-flop when both the inputs are 1.
3. Master-slave configuration is used in flip-flops to store 2-bits of information.
4. A transparent latch consists of a D type flip-flop.

Which of the above statements is/are correct ?

(A) 1 only (B) 1, 3 and 4
(C) 1, 2 and 4 (D) 2 and 3 only

MCQ 208

Which of the following flip-flop is used as a latch ?

(A) J-K flip-flop (B) R-S flip-flop
(C) T flip-flop (D) D flip-flop

MCQ 209

Which of the following conditions should be satisfied to call an astable multivibrator circuit using discrete components as a digital circuits ?

1. A flip-flop is always a digital circuit.
2. Only when we assign 1 and 0 to the high and low levels of the output, a flip-flop is called a digital circuit.

3. Only if the power supply voltage is maintained at +5 V or – 5 V, it is called a digital circuit.
4. Only if it is in IC form, following the technology of IC manufacture, it is called a digital circuit.

Select the correct answer from the codes given below :

(A) 1 only (B) 2 and 3

(C) 2 only (D) 3 and 4

MCQ 210

Which of the following circuits come under the class of sequential logic circuits ?

1. Full-adder
2. Full-subtractor
3. Half-adder
4. *J-K* flip-flop
5. Counter

Select the correct answer from the codes given below :

(A) 1 and 2 (B) 2 and 3

(C) 3 and 4 (D) 4 and 5

MCQ 211

Consider the following statements regarding registers and latches :

1. Registers are made of edge triggered FFs whereas latches are made from level triggered FFs.
2. Registers are temporary storage devices whereas latches are not.
3. A latch employs cross-coupled feedback connections.
4. A register stores a binary word whereas a latch does not.

Which of the above statements is/are correct ?

(A) 1 only (B) 1 and 3

(C) 2 and 3 (D) 3 and 4

MCQ 212

Which of the following capabilities are available in a Universal Shift Register ?

1. Shift left
2. Shift right
3. Parallel load
4. Serial add

Select the correct answer from the codes given below :

(A) 2 and 4 only (B) 1, 2 and 3

(C) 1, 2 and 4 (D) 1, 3 and 4

MCQ 213

Which of the following measurements can be done using a counter ?

1. Pulse duration
2. Interval between two pulses
3. Amplitude of the pulse
4. Rise time of a pulse

Select the correct answer from the codes given below :

(A) 1 and 2 (B) 2 and 3

(C) 1 and 4 (D) 2 and 4

MCQ 214

Match **List - I** (Type of N-bit ADC) with **List - II** (Characteristics) and select the correct answer using the codes given below the lists :

	List I		**List II**
a	Flash converter	1.	Integrating type
b	Successive approximation	2.	Fastest converter
c	Counter ramp	3.	Maximum conversion time $= N$ bits
d	Dual slope	4.	Uses a DAC in its feedback path

Codes :

	a	**b**	**c**	**d**
(A)	2	3	4	1
(B)	1	3	4	2
(C)	2	4	3	1
(D)	1	4	3	2

MCQ 215

In which one of the following types of analog to digital converters the conversion time is practically independent of the amplitude of the analog signal ?

(A) The dual slope integrating type

(B) Successive approximation type

(C) Counter ramp type

(D) Tracking type

MCQ 216

Assertion (A) :When all inputs of a NAND gate are shorted to get a one input, one output gate, it becomes an inverter.

Reason (R) : When all inputs of a NAND gate are at logic '0' level, the output is at logic '1' level.

(A) Both A & R are true and R is the correct explanation of A

(B) Both A & R are true but R is NOT the correct explanation of A

(C) A is true but R is false

(D) A is false but R is true

****